*Detail Proposal Form - Ideate Stage of Quarter Finals*

1. *Registration ID*

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1. *Name of Institute\**

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1. *Team Name\**

*The NANDs*

1. *Team Member Details\**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| *Name of Team Members* | *Email Id* | *Contact Number* | *Branch / Area of Specialisation* | *Name of Institute* |
| *Member 1 \** | *Sharan SK* | *8248762420* | *Computer Science and Engineering* | *Indian Institute of Information Technology,Design and Manufacturing* |
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1. *Faculty Details\**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Name of faculty* | *Email ID* | *Contact Number* | *Designation* | *Department Name* | *Name of Institute* |
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*Section-I: Hardware Resource Section*

1. *Name of Hardware Resources \**

*SHAKTI Vajra (C64-A100) on Artix7-100T FPGA,*

*If selected Hardware Resources with ARTIX7-100T FPGA, then provide justification for not making use of the Hardware Resources with Artix7-35T FPGA, which may result in an optimal utilization of the Hardware Resources for the innovative solution proposed. (if not applicable put N/a)*

|  |
| --- |
| *Artix-7 100T is preferred as we made design plans for Shakthi Vajra Processor which is offered only with artix-7 100T and also it offers large number of logic resources which are important for a network processor* |

*If selected Hardware Resources as other (FPGA Board other than Artix7-35T and Artix7-100T), then please mention the details of FPGA Board of your choice ( like Name of Vendor, Series etc.). ( If not applicable put N/a)*

|  |
| --- |
| *N/A* |

*If selected Hardware Resources as Other ( FPGA Board other than Artix7-35T and Artix7-100T) then select processor eco system of your choice among SHAKTI – E32, SHAKTI- C64, VEGA ET1031 or VEGA AS1061. (if not applicable put N/a)*

|  |
| --- |
| *N/A* |

*Section-II: Technical Aspects of Innovative Solution*

1. *Proposal Title:*

*Embedded Processor for Network System Design*

1. *Proposal Summary*

*The number of users connected to the Internet is significantly increasing. As a result, the number of packet processing per second is also increasing to meet the demand. The network system's design encompasses various network functions implementation such as error checking, IP lookup, packet classification, fragmentation, segmentation, etc. Network system design implemented using a network processor where the network processor is a technology. It uses a set of the embedded processor to process the lower layer processing in the network. The objective of this work is to implement the following list of network functions: Address lookup and packet forwarding, Error detection and correction, Fragmentation, segmentation, and reassembly, Frame and protocol demultiplexing, Packet classification, Queueing and packet discard, Scheduling, and timing, Security: authentication and privacy, Traffic measurement and policing and Traffic shaping. It also estimates the performance of each function on the embedded processor.*

*This proposal aims to estimate the performance of the processor against the network functions. The software implementation of network functions is estimated. This proposal's use cases are network processors, network systems such as switches, routers, and firewalls.*

1. *Please provide a concept note explaining the technology/ technical & other necessary details*

Layer 2 address lookup and IP lookup are one of the time consuming network functions. As part of this proposal we will buffer the packet on the available Block RAMs and extract the header information. The extracted header information is used as an input to the SHAKTI core and it will perform the address lookup for Layer 2 and IP lookup for layer 3. Lookup algorithms are typically a search algorithm, which can be performed in software approach using binary Trie and hardware point of you it will be implemented using associative memory or using the TCAM. As part of this work we will perform software based lookup.

1. *Briefly state the Objectives and Proposed Approach*

*[Describe how the proposed innovation addresses the problem. Clarify the current status of the innovation]*

*The description should cover the following points:*

*1). Strategy and/or methodology of work.*

IP lookup and address lookup will be implemented using the software running on the SHAKTI core. The incoming packet is buffered on the existing Block RAM of the FPGA and extracted header information will be passed to SHAKTI core, where address lookup and IP lookup will be performed based on the software implementation.

*2). Block Diagram/ images highlighting all the subsystems and supported with a broad details of each block/subsystem.*

The generic block diagram of the proposed system is shown in the Fig.1. The subsystems are Packet Buffer and Packet parser. The packet buffer is implemented using the available Block RAM. The buffered packet header is parsed and the extracted header information is fed to SHAKTHI core. Where address lookup of layer 2 and IP lookup of layer 3 is implemented on SHAKTI core.

Block RAM

Packet Buffer

Header Parser

FPGA Prototype Board

Incoming Packet

Extract the

Packet Header

SHAKTI Core

Next Hop

Lookup

Fig. 1 Generation of Block Diagram

*3). Scope and boundaries of the work, including any issues that will not be covered.*

As part of this proposal we are implementing only layer 2 address lookup and layer 3 IP lookup. Though there are additional network functions are available. We would like to scope our work related to core network function is lookup.

*4). Data analysis (sample size, data collection)*

NOT APPLICABLE

1. *Has any preliminary work been carried out?*

*Give status of work done earlier and its timelines. If yes, please provide the background details.*

Yes, we have done the preliminary work related to the proposal as part of research work and we have published research articles related to this work. We have published researched articles in the reputed journals related to IP lookup and packet classification.

1. *Timelines*
2. *Quarterly timelines vis-a-vis activities*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | QUARTER 1 | | | QUARTER 2 | | |
|  | M1 | M2 | M3 | M4 | M5 | M6 |
| Block RAM based Packet Buffering | M1 | M1 |  |  |  |  |
| Packet Parser implementation | M1 | M2 |  |  |  |  |
| Layer 2 Address lookup |  | M2 | M3 |  |  |  |
| Layer 3 IP lookup |  | M2 | M3 |  |  |  |
| SHAKTI Core Implementation |  |  | M3 | M4 |  |  |
| Software implementation |  |  |  | M4 | M5 |  |
| Demonstration |  |  |  |  |  | M6 |

1. *Factually verifiable Indicators or Physical deliverables or Output indicators*

* BlockRAM initialization and for Packet Buffer
* Packet Parser Implementation
* Layer 2 Address lookup Algorithm
* Layer 3 IP lookup Algorithm
* Network processing function – lookup on SHAKTI Core

1. *Intellectual Property*

*Does the applicant or the applicant company own any IP related to this project. If yes, give details. (Please mention Patent Number, Patent Title and Patent Assignee)*

NIL

1. *Requirement of Equipment/ Accessories/ Components/ Resources other than the Hardware Resources provided under the Challenge*
2. *Requirement Equipment/ Accessories/ Components*
3. *Quantity*
4. *Estimated Value*

The FPGA prototype board is supplied as part of the grant and SHAKTI core. The existing hardware resources on the FPGA board is sufficient to implement and demonstrate lookup on SHAKTI Core.

*NO Fund is required.*

1. *Relevant References.*

* S. Veeramani and Sk Noor Mahammad, "Efficient IP lookup using hybrid trie-based partitioning of TCAM-based open flow switches", Journal of Photonic Network Communications, Springer Publisher, Vol.28, no. 2, pp.135-145, October 2014. [SCI Indexed]
* Shanmugakumar Murugesan and Noor Mahammad Sk, "A Novel Range Matching Architecture for Packet Classification without Rule Expansion", ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), Vol. 23, no. 1, pp. 8:1-8:15, September 2017. [SCI Indexed]
* Veeramani S, Manas Kumar, and Sk Noor Mahammad, "Hybrid Trie based Partitioning of TCAM based Openflow Switches", in the proceedings of 7th IEEE International Conference on Advanced Networks and Telecommunications Systems (ANTS), pp. 1-5, Chennai, December 2013.
* Veeramani S, S Rahul Sharma and Sk Noor Mahammad, "Constructing scalable hierarchical switched openflow network using adaptive replacement of flow table management", in the proceedings of 7th IEEE International Conference on Advanced Networks and Telecommunications Systems (ANTS), pp. 1-3, Chennai, December 2013.
* Veeramani S, Biraja Nalini Rout, and Noor Mahammad Sk, "Novel Approach to Secure Channel using C-SCAN and microcontroller in Openflow", in the proceedings of 7th IEEE International Conference on Advanced Networks and Telecommunications Systems (ANTS), pp. 1-4, Chennai, December 2013.

*Section-III: Business Aspects of Innovative Solution*

1. *Novelty*

*[Explain how your idea is innovative and how it is different from the existing products/solutions in the markets or current state-of-the-art. Competitive advantage of the proposed solution may be elaborated)*

*One of the common things that many network processors carry is its ability to Multiprocess. The uniqueness our product lies in the execution of it. From our abstract it should be pretty much clear on the variety of functions that it can support and execute and comparing those functionalities with those of an embedded processor, can boost the performance much better. Moreover, one other advantage is the processor's nativity, our country is yet to grab the fullest potential of the Network Processor Market, Using these kinds of processors can help in maintaining the large traffic in the networking industry.*

*Although there are network processors for high-speed networks, no processor is available that considers the requirements of the interface between networks of a service provider and a customer. While each individual task of a network processor is well understood, it is unclear how different tasks, that potentially show interfering properties, should cooperate to preserve the service quality. We propose a new scheme for network services that has been derived from the requirements of multi-service access networks. The scheme combines the advantages of existing services by providing quantitative guarantees for flows in terms of loss and delay, in-order delivery, graceful service degradation, and qualitative guarantees for aggregates of flows to enable resource sharing.*

1. *Opportunity*

*[What is the requirement and potential societal & market impact? ]*

*The markets for network processor are intensely competitive ,rapidly evolving and are subjected to rapid technological changes.*

*In recent days we could see the importance of one of the fastest-growing industry: Network Processor Market. It is estimated that nearly 49% of the market share is owned by Network processor Market in 2016. In 2019,The global Network Processor market size was $3712.2 million and is expected to reach $9339.6 million by 2026.Its main advantages is its wide range of applications.Network Processors are employed in the manufacturing of routers ,network switches,packet inspection,session controllers,firewall,transmitter devices ,etc.Moreover one other advantage is the processor's nativity,our country is yet to grab the fullest potential of the Network Processor Market,Using these kind of processors can help in maintaining the large traffic in networking industry .*

1. *Market Feasibility*

*[What is the addressable Market and the Target Market and the Competitor Landscape]*

The addressable market can be considered as the many existing network devices, with a main focus on hardware firewalls. This is in extensive use by ISP’s for filtering traffic and blocking unauthorized access. Presently CISCO has a large market share worldwide. However there are many much smaller companies also existing in the same market meaning entering the market should be relatively easy. Further as the market is rapidly expanding in India it would definitely be possible to gain a significant market share by bringing in cost based differentiation. The rapid expansion of the market means that this is the ideal time to bring a SWADESHI company into the scene.

1. *Commercialization Roadmap*

*What do you envision to be the key next step to making an impact with this innovation/ commercialize this innovation ? {(e.g., Sponsored research support, Licensing, Venture Financing) What is the time frame? Commercialization plan should indicate: 1). Market entry strategy & roadmap for scalability. 2). Timelines and Milestones. 3). Data analysis (sample size, data collection)*

NOT APPLICABLE – INSTITUTE PROJECT – PROOF OF CONCEPT DEMO

1. *Challenges or Risk factors associated with the project and the proposed mitigation strategies*

*There are no Risk Factors involved with the project.*

1. *Have you established the Link-up with any agency/ organization, other than the Team members, for joint- development of this innovative solution.*

*No,For Now We are exploring opportunities*

1. *Have you received any interest from the end user of this innovative solution*

*[Share details, Annex the Letter of interest received]*

*Not yet*

1. *Have you approached any other organisation/agency for financial support for the present activity? Please give details*
2. *Relevant References.*